A COMPACT BROADBAND, SIX-BIT MMIC PHASOR WITH INTEGRATED DIGITAL DRIVERS+

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ABSTRACT

Digital and microwave technologies have been successfully combined on a single chip to realize a broadband, 6-bit MMIC phase shifter. It exhibits low insertion loss, good VSWR, and exceptional phase performance with less than 3 degrees RMS phase error for all sixty-four phase states over the entire 7.2-10.2 GHz band. Compared to previous designs, the number of required control lines has been reduced by a factor of two due to the integration of the digital driver circuitry.

INTRODUCTION

The microwave control component employed to realize the phase shift function in an electronically scanned array is the phase shifter. This component provides the phase control necessary at each array element for pattern generation and beamsteering. In airborne applications where the transmit/receive (T/R) module is densely integrated the phase shifter must, in addition to exhibiting good microwave performance, be small, consume minimal power, and require as few control lines as possible.

This paper describes a six-bit phase shifter with integrated digital drivers that eliminate 6 of the 12 control lines normally required in the already crowded T/R module environment. This compact phase shifter (2.9 mm x 2.9 mm x 0.1 mm) achieves low RMS phase error, a low overall insertion loss with minimal variation, and a low VSWR over all 64 phase states in the design band of 7.2-10.2 GHz. In fact, performance is more than adequate over a wider band.

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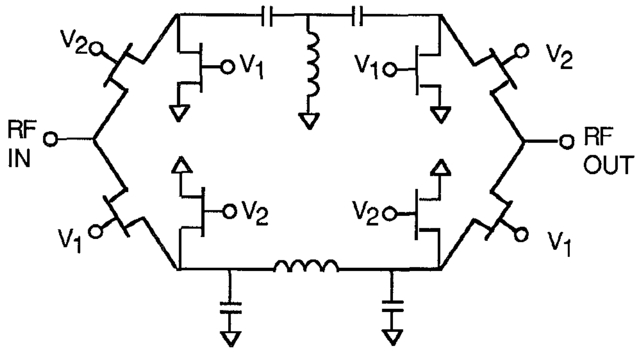
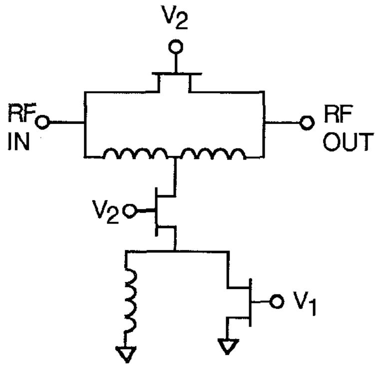
In order to be easily integrated with the existing phase bits without requiring an increase in chip size, the digital drivers have to be extremely small. Each digital driver is 150 x 30 microns; a significant reduction in size over previously reported designs[1]. Low dc power consumption is another essential feature of the drivers when one considers that six drivers are required per chip. To keep consumption low, digital FET widths as small as 4 microns were fabricated, whereas the RF FETs required widths as large as 950 microns. Total dc power consumption for the combination of all six phase bits and their respective drivers was less than 85 mW.

PHASE SHIFTER DESIGN

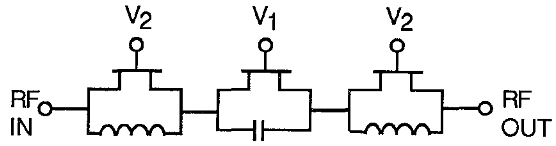
The phase shifter circuit consists of six digital bits corresponding to differential phase shifts of 180, 90, 45, 22.5, 11.25, and 5.625 degrees cascaded in a linear arrangement. This provides 64 phase states between 0 and 360 degrees in increments of 5.625 degrees. The 180, 90, and 45 degree phase bits are of the switched line type consisting of π or T-type highpass/lowpass phase shift networks and two single pole double throw (SPDT) FET switches[2]. Included in these bits are tunable inductive and capacitive elements to provide the capability of fine tuning the phase bit performance. The 22.5, 11.25, and 5.625 degree phase bits are of the embedded-FET type, where the FET switches become part of the phase shifting highpass/lowpass network[3]. Schematics for these circuits are shown in Figure 1. All bits are controlled by two complementary signals, 0 volts and the pinch-off voltage, Vp. The switching is performed through 2 Kohm resistors which provide RF isolation between the gates and the control sources. In the design of the phase shifter, each phase bit was optimized to have a minimum 15 dB return loss so that interactions between individual bits in the complete phase shifter were minimized. The



(a) 180, 90, and 45 Degree Bits



(b) 22.5 Degree Bit



(c) 11.25 and 5.625 Degree Bits

Figure 1. Phase Bit Schematic Diagrams

individual bits were designed and simulated on TOUCHSTONE™ (EESOF) and layout was performed on CHIPGRAPH™ (MENTOR). The phase shifter chip is shown in Figure 2.

DIGITAL DRIVER DESIGN

The driver, an inverter from the Unbuffered FET Logic family, is fabricated using N-channel depletion mode MESFETs[4]. A schematic and a photograph are shown in Figures 3 and 4. The driver accepts CMOS type input signals and operates between 5 and -5.6 volt supplies. The circuit was designed to operate with minimal power consumption, have rise and fall times of approximately 10 ns and occupy minimal chip area. These objectives had to be met without any modifications to the existing microwave process. To meet these objectives, very small geometry devices with 4 micron gate widths were used for the driver circuit.

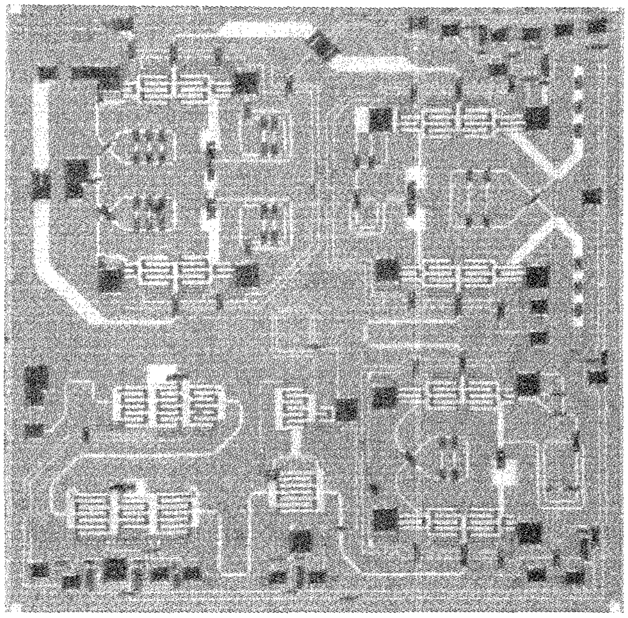


Figure 2. Photograph of 6-Bit Phase Shifter With Drivers

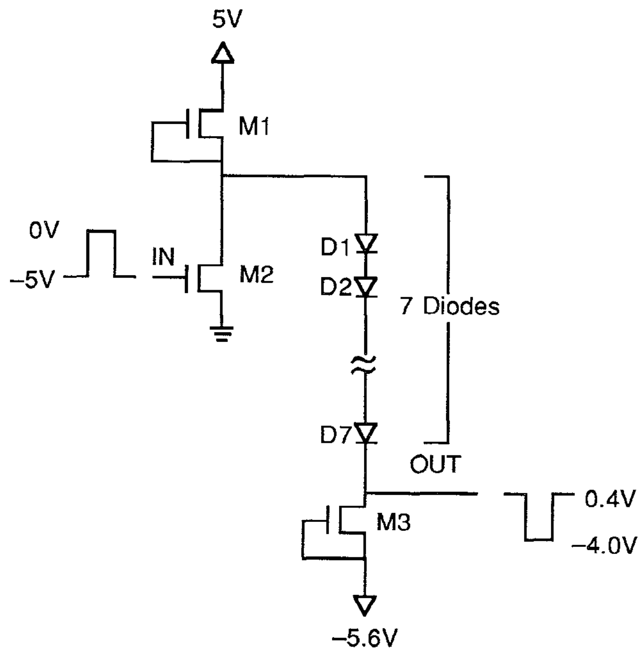


Figure 3. Driver Schematic Diagram

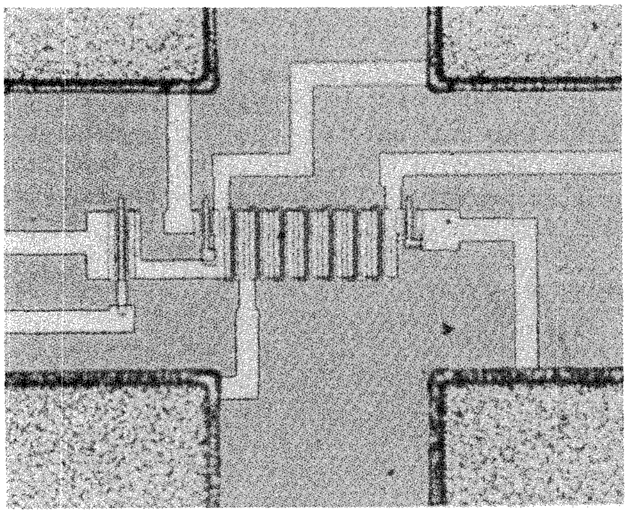


Figure 4. Photograph of Driver Circuit

The FETs were characterized and model parameters extracted from I-V characteristic curves. Simulations of various designs were performed using a SPICE type simulator. Figure 5 is a plot of the simulated input/output waveforms. The load for this circuit simulation is a 1 pf capacitor.

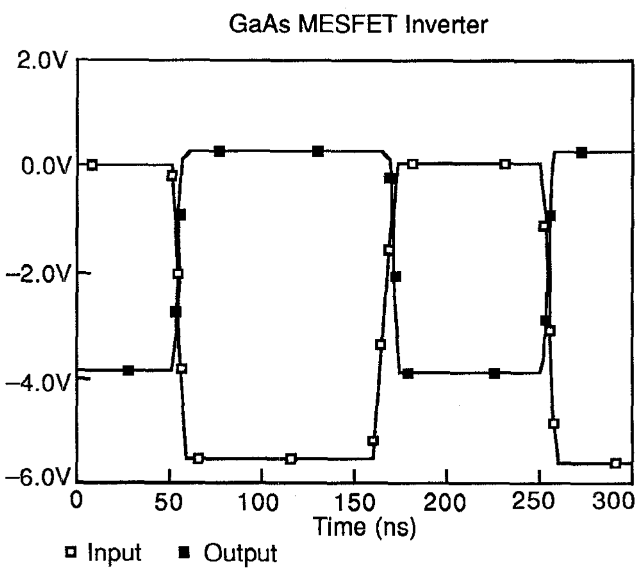


Figure 5. Simulation of Driver Circuit Response

In addition to the driver, several test structures were fabricated. A ring oscillator was included to characterize the performance of each lot and to obtain data to improve the device model. Several discrete devices were fabricated, some with 2 micron gate widths. These devices were used for obtaining statistical and performance data.

PERFORMANCE

The 6-bit phase shifter with digital drivers was measured with a computer controlled Hewlett Packard 8510 automatic network analyzer (ANA) connected to a Cascade Microtech probe station. An in-house test program automatically switches and records S-parameters for all 64 phase states.

The measured response of all 64 phase states over the 7-11 GHz band is summarized in Figures 6 through 8. For the reference state, all phase bits were switched to the highpass state. RMS phase error is less than 3 degrees. Minimum return loss is 13 dB with an overall mean return loss of 20 dB. RMS insertion loss deviation is less than 0.5 dB with an overall mean loss of 9 dB.

The digital driver performance was similar to the computer simulation. A 0 volt to -5.0 volt signal at the input was inverted to -4.0 and +0.4 volts at the output. dc power dissipation was 13.6 mW, and propagation delay through the driver was 180 ps.

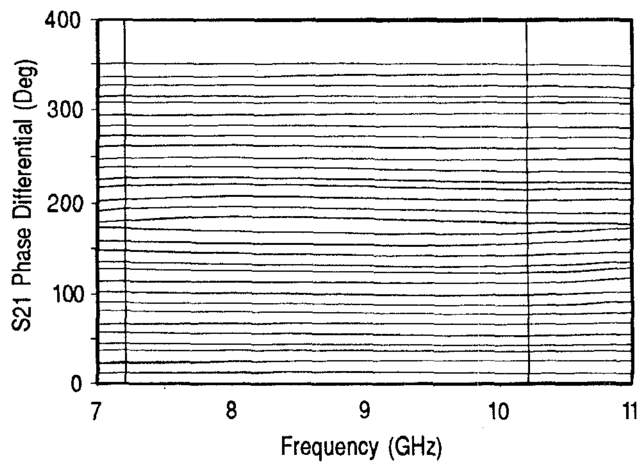


Figure 6. Measured Phase Differential of 32 States

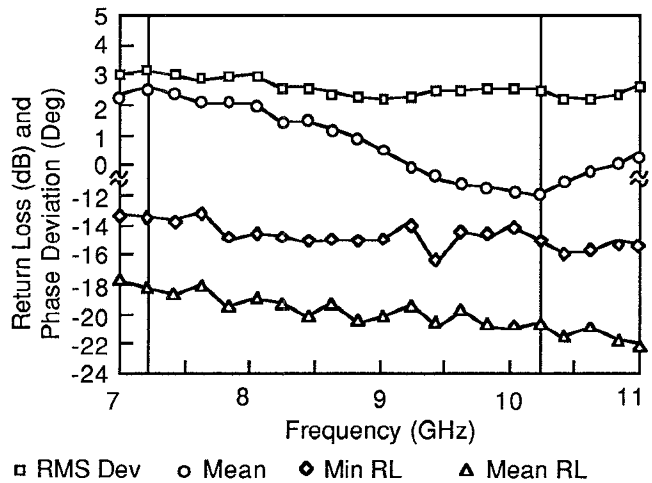


Figure 7. Measured Phase Deviation and Return Loss of 64 States

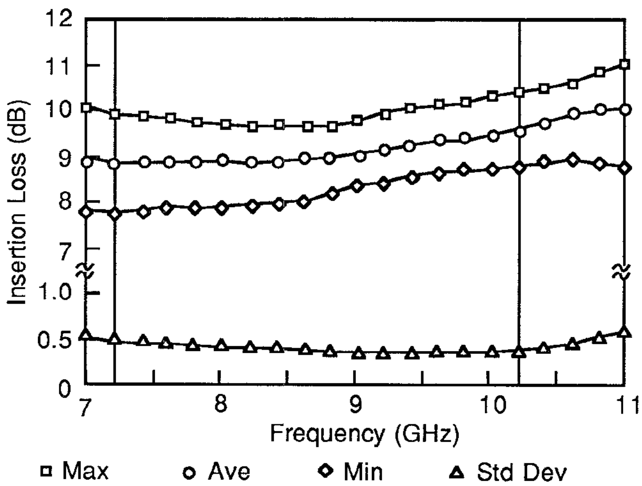


Figure 8. Measured Insertion Loss of 64 States

FABRICATION

The phase shifter was processed at the Hughes Microwave Products Division foundry in Torrance, CA using their standard gain process. Because the digital drivers were added to an already complex circuit, 1 micron gate lengths were used to ensure a high yield. Total gate periphery on the chip is 12.9 mm with FETs as large as 950 microns directly adjacent to FETs as small as 2 microns–a significant processing accomplishment.

CONCLUSION

Digital drivers have been successfully integrated on a high performance broadband digital phase shifter thus reducing the control requirements in a dense T/R module environment. This has been done without degrading RF performance, increasing chip size, or substantially increasing power consumption. Such a chip is required in T/R channels for airborne active array radars.

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